(12) UK Patent Application (19) GB (11) 2 350 721 (13) A

(43) Date of A Publication 06.12.2000

(21) Application No 9920048.7

(22) Date of Filing 24.08.1999

(71) Applicant(s)
Arima Optoelectronics Corporation
(Incorporated in Taiwan)
6th Floor, No 327, Sung Lung Road, Taipei, Taiwan

(72) Inventor(s)
Wang Nang Wang
Yurii Georgievich Shreter
Yurii Toomasovich Rebane
Boris Samuilovich Yavich
Vladislav Evgenievich Bougrov

(74) Agent and/or Address for Service
Page Hargrave
Southgate, Whitefriars, Lewins Mead, BRISTOL,
BS1 2NT, United Kingdom

(51) INT CL[7]
H01L 21/20

(52) UK CL (Edition R)
H1K KLDX K2R3A K2S1B K2S1C K2S1D K2S1E K2S16 K9C2 K9C3 K9E K9N3

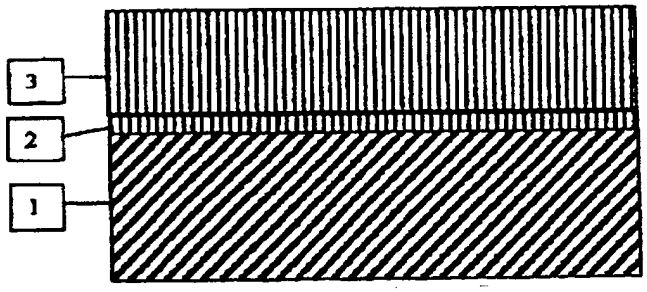
(56) Documents Cited
WO 99/25030 A1 **WO 93/26049 A1** **US 5232862 A**

(58) Field of Search
UK CL (Edition Q) **H1K KLDBA KLDBB KLDBM KLDBT KLDBX KLDX**
INT CL[6] **H01L**
ON LINE,W.P.I.,EPODOC,JAPIO

(54) Abstract Title
Growing semiconductor layers

(57) A method of growing a Group III-nitride semiconductor layer 3 on a lattice mismatched substrate 1 comprises depositing an amorphous or polycrystalline buffer layer 2 of $B_xAl_yGa_zIn_{1-x-y-z}N$ alloy on the substrate and recrystallizing the buffer layer before epitaxially growing the semiconductor layer. The substrate may comprise sapphire and the semiconductor layer may be GaN.

Fig. 1c



GB 2 350 721 A

Fig.1a

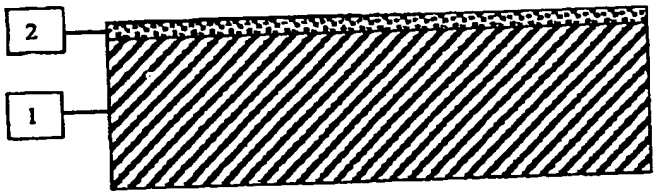


Fig.1b

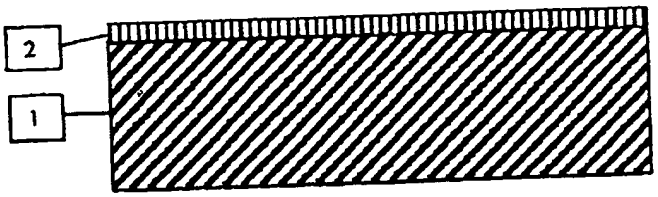


Fig.1c

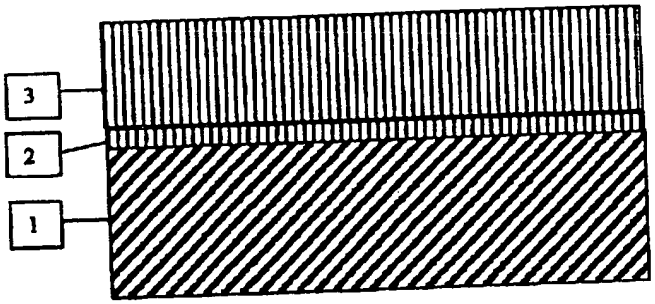


Fig.2a

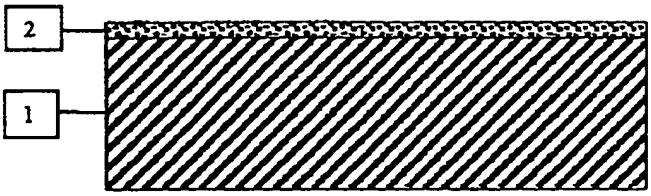


Fig.2b

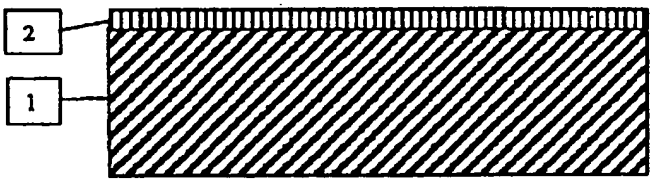


Fig.2c

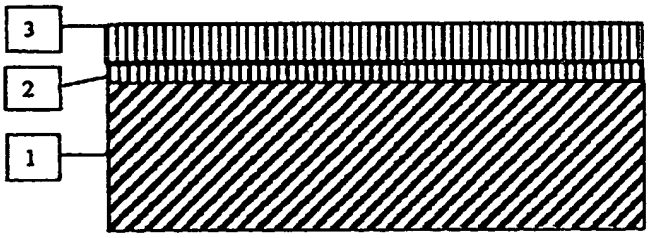


Fig.2d

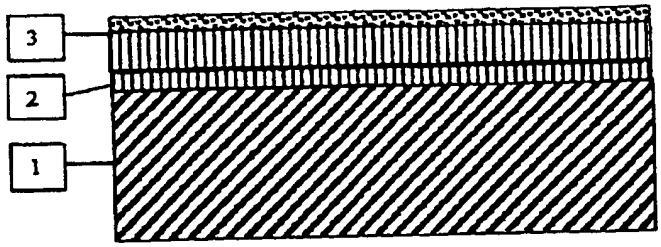


Fig.2e

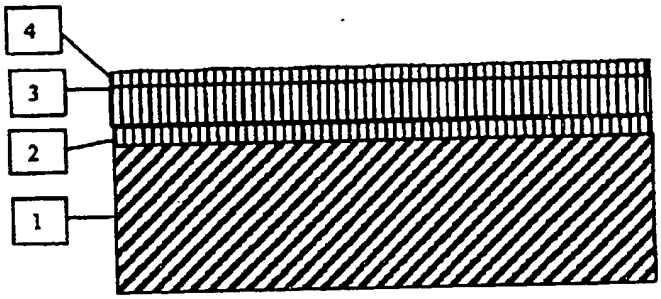
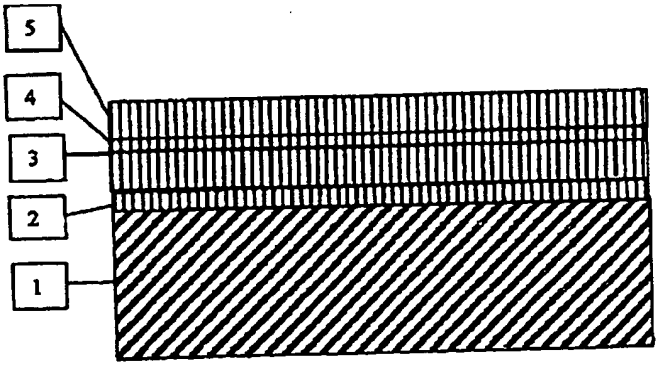


Fig.2f



EPITAXIAL GROWTH METHOD OF III- NITRIDE SEMICONDUCTORS ON HIGHLY MISMATCHED SUBSTRATES WITH USE OF $B_xAl_yGa_zIn_{1x-y-z}N$ BUFFER NUCLEATION LAYER

BACKGROUND OF THE INVENTION

1.Field of the Invention

The present invention generally relates to fabrication of III-nitride semiconductor devices by growth of epitaxial semiconductor layers on highly lattice mismatched substrates. More particularly, the invention deals with a special buffer nucleation layer which accommodates high mismatch.

2. Description of the Prior Art

Epitaxial growth of III-nitride semiconductor on highly mismatched substrates results in extremely strained semiconductor layers. This strain gives rise to the formation of many extended defects such as dislocations, grain boundaries, stacking faults, inversion domains etc., and it is generally responsible for the poor quality of the grown semiconductor layers. Buffer nucleation layers have been used during several decades for the strain reduction and improving quality of the grown semiconductor layers. Usually buffer nucleation layers for epitaxial growth of III-nitride semiconductor on highly mismatched substrates are made of AlN, GaN compounds or $Al_xGa_yIn_{1-x-y}N$ alloys.

The present invention employs the buffer nucleation layer made of boron containing $B_xAl_yGa_zIn_{1x-y-z}N$ alloys.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a growth method that allows to eliminate the strain resulting from high

mismatch between the lattice parameters of the III-nitride semiconductor and a substrate on which this semiconductor is grown.

This invention states the use of the boron containing $B_xAl_yGa_zIn_{1x-y-z}N$ alloy buffer nucleation layer in the growth process of III-nitride semiconductors on highly lattice mismatched substrates.

Providing boron containing alloys as materials for depositing nucleation layers increases density of nuclei. The boron containing alloys have higher crystallization temperature comparing to III-nitride alloys without boron. The higher crystallization temperature results in lower mobility of adsorbed atoms over the surface of the substrate. This leads to higher density of nuclei in the nucleation layer and smaller nuclei sizes. After the recrystallization of the buffer nucleation layer this results in improved structural quality of epitaxial layers.

The high chemical activity of boron atoms compared with other III-group elements is also favorable for the formation of higher density of nucleation sites.

The other advantage of boron containing alloys in the buffer nucleation layer is the admixture of BN graphite phase which reduces the hardness and increases the plasticity of the buffer nucleation layer that in turn results in better strain relaxation of III-nitride epilayers grown on highly mismatched substrates.

Using $B_xAl_yGa_zIn_{1x-y-z}N$ alloys comparing with AlN, GaN compounds or $Al_xGa_yIn_{1-x-y}N$ alloys, provides wider range of lattice constant variation and wider possibility for mismatch reduction for various substrates.

The growth process with use of the buffer layer consists of the following main three stages.

1. The thin amorphous or polycrystalline buffer nucleation layer is deposited on the substrate at the temperature in the range 300 - 800 C.

2. Then a recrystallization of the buffer nucleation layer at temperature 1000 - 1500 C is performed.
3. Then the epitaxial III-nitride semiconductor layer is grown on the recrystallized buffer nucleation layer at temperature 700 - 1500 C.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1a-c, illustrates the use of the boron containing $B_xAl_yGa_zIn_{1x-y-z}N$ alloy buffer nucleation layer in the growth process of III-nitride semiconductors on highly lattice mismatched substrates.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments of the present invention are illustrated in Figs. **1a-c**. These figures show the principal stages of the growth of the epitaxial semiconductor layer using the boron containing $B_xAl_yGa_zIn_{1x-y-z}N$ alloy buffer nucleation layer.

At first stage, shown in Fig.**1a**, the amorphous or polycrystalline buffer nucleation layer **2** with the thickness from 5 Å to 500 Å is deposited on the substrate **1** at temperature in the range 300 - 800 C.

At second stage, shown in Fig.**1b**, a recrystallization of the buffer nucleation layer **2** at temperature 1000 - 1500 C is performed.

At third stage, shown in Fig.**1c**,the epitaxial III-nitride semiconductor layer is grown on the recrystallized buffer nucleation layer at temperature 700 - 1500 C.

The advantages of using boron containing $B_xAl_yGa_zIn_{1x-y-z}N$ alloys in the buffer nucleation layer are:

1. Boron containing alloys as materials for depositing nucleation layers reduce nuclei sizes and increase density of nuclei. After the recrystallization of the buffer nucleation layer, this results in improved structural quality of epitaxial layers.

2. The high chemical activity of boron atoms compared with other III-group elements is also favorable for the formation of higher density of nucleation sites.
3. The admixture of BN graphite phase reduces the hardness and increases the plasticity of the buffer nucleation layer that in turn results in better strain relaxation of III-nitride epilayers grown on highly mismatched substrates.
4. $B_xAl_yGa_zIn_{1-x-y-z}N$ alloys comparing with AlN, GaN compounds or $Al_xGa_yIn_{1-x-y}N$ alloys, provide wider range of lattice constant variation and wider possibility for mismatch reduction for various substrates.

Thus, the use of the boron containing $B_xAl_yGa_zIn_{1-x-y-z}N$ alloy buffer nucleation layer allows to grow the high quality epitaxial III-nitride semiconductor layers on highly mismatched substrates.

The invention will be more fully understood by reference to the following examples

EXAMPLE 1

At first stage, shown in Fig.**1a**, the buffer nucleation layer **2** of $B_{0.1}Ga_{0.9}N$ alloy with the thickness 200 Å is deposited on the sapphire substrate **1** at temperature 500 C.

At second stage, shown in Fig.**1b**, the temperature is risen up to the growth temperature 1000 C of the GaN semiconductor layer. The temperature rise causes recrystallization of the buffer layer **2** as shown in Fig.**1b**.

Then 2 μm thick GaN epitaxial layer **3** is grown on the recrystallzed layer **2**.

EXAMPLE 2

At first stage, shown in Fig.**2a**, the first buffer nucleation layer **2** of $B_{0.1}Ga_{0.9}N$ alloy with the thickness 200 Å is deposited on the sapphire substrate **1** at the temperature 500 C.

At second stage, the temperature is risen up to the growth temperature 1000 C of the GaN semiconductor layer. The temperature rise causes recrystallization of the first buffer layer **2** as shown in Fig.**2b**.

At the third stage, temperature is risen up to the temperature 1150 C to grow the 500 Å thick intermediate GaN epitaxial layer **3** as shown in Fig.**2c**.

Then, the second buffer nucleation layer **4** of $B_{0.1}Ga_{0.9}N$ alloy with the thickness 200 Å is deposited on the first GaN epitaxial layer **3** at the temperature 500 C as shown in Fig.**2d**.

After that, the temperature is risen up to the growth temperature 1000 C for recrystallization of the second buffer nucleation layer **4** c.

Finally, then 2 μm thick the GaN epitaxial layer **5** is grown on the second buffer nucleation layer **4** as shown in Fig.**2f**.

EXAMPLE 3

At first stage, shown in Fig.**1a**, the buffer nucleation layer **2** of $B_{0.1}Ga_{0.9}N$ alloy is deposited on the sapphire substrate **1** simultaneously with temperature rise from 600 C up to 1000 C with the rate of temperature variation 5 C per second.

At second stage, shown in Fig.**1b**, the 2 μm thick GaN epitaxial semiconductor layer **3** is grown on the recrystallized buffer nucleation layer **2**.

CLAIMS

1. An epitaxial growth method of III-nitirde semiconductor layers and structures on highly mismatched substrates using the $B_xAl_yGa_zIn_{1-x-y-z}N$ alloys in the buffer nucleation layer comprising:

the deposition on a substrate of the amorphous or polycrystalline buffer nucleation layer with the thickness from 10 Å to 1000 Å at the temperature in the range 300 - 800 C;

the recrystallization of the buffer nucleation layer at temperature 1000 - 1500 C during the time period in the range 5 - 500 sec;

the epitaxial growth of a III-nitride semiconductor layer or structure on the recrystallized buffer nucleation layer at the temperature 700 - 1500 C.

2. The buffer nucleation layer made of ternary $B_xAl_{1-x}N$ alloys, where $0<x\leq1$.

3. The buffer nucleation layer made of ternary $B_xGa_{1-x}N$ alloys, where $0<x\leq1$.

4. The buffer nucleation layer made of ternary $B_xIn_{1-x}N$ alloys, where $0<x\leq1$.

5. The buffer nucleation layer made of $B_xAl_yGa_zIn_{1-x-y-z}N$ alloys, where $0<x\leq1$, $0\leq y\leq1$, $0\leq z\leq1$, $x+y+z\leq1$.

6. An epitaxial growth method of III-nitirde semiconductor layers and structures on highly mismatched substrates using the $B_xAl_yGa_zIn_{1-x-y-z}N$ alloys in the buffer nucleation layer comprising:

the continuos deposition on a substrate of the amorphous or polycrystalline buffer nucleation layer with the thickness from 50 Å to 1000 Å at the rising temperature from 300 - 800 C to . 800 - 1500 C with the temperature rising rate in the range from 1 - 10 degree per second.

the epitaxial growth of a III-nitride semiconductor layer or structure on the recrystallized buffer nucleation layer at the temperature 700 - 1500 C.

7. The use for the epitaxial growth of III-nitride semiconductor of 1 to 10 buffer nucleation layers made of $B_xAl_yGa_zIn_{1-x-y-z}N$ alloys, where $0<x\leq 1$, $0\leq y\leq 1$, $0\leq z\leq 1$, $x+y+z\leq 1$ with intermediate epitaxial III-nitride semiconductor layers.

The Patent Office

8

INVESTOR IN PEOPLE

Application No: GB 9920048.7 **Examiner:** COLIN STONE
Claims searched: All **Date of search:** 6 December 1999

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q): H1K(KLDBA,KLDBB,KLDBM,KLDBT,KLDBX,KLDX)

Int Cl (Ed.6): H01L

Other: ON LINE,W.P.I.,EPODOC,JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	WO93/26049 A1	APA OPTICS (See page 4 line 35-page 5 line 6)	2-5
X	US 5232862	GENERAL MOTORS	2-5

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.